REMARKS

Claims 1-6 are pending in the application. Claims 1-5 are rejected. Claim 6 is objected to but would be allowable if placed in independent form. Applicant has amended claims 1 and 2.

Claim Rejections - 35 U.S.C. § 102

Claim 2 is rejected under 35 U.S.C. § 102(e) as being anticipated by Asada et al (6,483,791). This rejection is traversed for at least the following reasons.

The present invention concerns a clock generator, which is particularly adapted to eliminate problems from high speed microprocessors due to undesired radiation noise (EMI). As explained at pages 1-3 of the present specification with regard to an illustrative but non-limiting embodiment that incorporates the invention, one approach to solving this problem is to use a spectrum spread clock, which incorporates a buffer memory of the type illustrated in Fig. 10. In order to reduce costs and eliminate the buffer memory, the Applicant's clock generator will generate a spectrum spread modulation clock which is capable of reducing the level of undesired radiation energy, and eliminates the need for buffer memory.

To this end, with respect to at least the embodiment illustrated in Fig. 1, the clock generator comprises a delay sync circuit 10 and a delay setting circuit 11. The delay sync circuit 10 includes a variable delay circuit 2 composed of plural delay elements that delay the reference clock, a phase comparator 3 that compares the phases of the reference clock and a delayed clock from the delay circuit 2, a first charge pump 4 that controls an inflow current and outflow current according to an output from the phase comparator 3 and a filter 5 that receives a current from the first charge pump. The output of the filter 5 is fed back to the variable delay circuit 2 as the delay control voltage D_{ctrl}.

Claim 2 specifically recites a clock generator comprising a phase control means that responds to an input reference clock and generates a phase controlled spread spectrum clock. The phase control means is specifically defined as varying a setting condition to spread a spectrum of the output clock.

The patent to Asada et al concerns a optical disk apparatus having a laser drive integrated circuit of the type illustrated in Figs. 1-3, where a laser drive integrated circuit 27 includes a waveform decoder 14. Fig. 40 illustrates an embodiment of the wave form decoder 14, which includes a change point timing generator 1407, as explained beginning at col. 22, line 37 and as illustrated in Fig. 46.

The change point timing generator will generate the timing of a change point corresponding to case packet signals CP-1 and CP-2 of an operation packet register 1402. The change point timing generator 1407 is supplied with the case packet (CP) signals via switch 1408. The generator also receives a channel clock (chCLK) and outputs a change point timing signal CP_trg. The change point timing generator 1407 controls the selector 1409 based on the CPtrg signal corresponding to CP-1 and causes the selector 1409 to output the L-1 signal of the operation packet register 1402. Upon receipt of the CP_trg signal corresponding to CP-2, the selector 1409 outputs L-2.

Clearly, there is no teaching or suggestion in the foregoing disclosure with regard to the desirability or achievement of spectrum spread modulation. The details of circuit 1407 are illustrated in Fig. 46 and are described at col. 25, line 13 - col. 26, line 20. As already noted, one input to the change point timing generator 1407 is a channel clock chCLK and the other is a case packet signal CP, with the only output being a case packet trigger CP_trg. Again, nothing in this disclosure concerns a spectrum spread modulation feature or the generation of a clock having such feature.

The subject matter of the invention, particularly as recited in claim 2, is not anticipated by Asada et al, since express limitations of the claim with regard to spectrum spread modulation are missing. Thus, the rejection should be overcome. Since the rejection may be based on a misunderstanding of the invention, Applicants have amended claim 2 to more clearly set forth the subject matter of the clock generator invention.

Claim Rejections - 35 U.S.C. § 103

Claims 1 and 3-5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Asada et al (6,483,791) in view of Lofgren et al (4,922,141). This rejection is traversed for at least the following reasons.

The Examiner relies upon his analysis of Asada et al to find the limitations recited in the clock generator of claim 1, specifically, the a phase control means as identically recited in claim 2. The Examiner admits that Asada et al does not teach a oscillator for generating a reference clock, as recited in the claim. However, the Examiner looks to Lofgren for an oscillator 10 that generates a reference clock. The Examiner asserts that it would be obvious to configure Asada et al with an oscillator for generating a reference clock so that the oscillator would provide a delay line with precise desired delays.

However, Applicants again note that Asada is not concerned with the use of a reference clock nor the generation of a spectrum spread modulation clock. Even within the environment of Asada et al, the Examiner would be using hindsight to find any reason for providing a reference clock for the structure in Fig. 46. The chCLK signal is not a "reference clock" signal as characterized by the Examiner, but is a clock related to channel presence and operation. In short, given the purpose of the disclosed circuit in an optical disk apparatus, there is simply no need for a reference clock or an output that is a spectrum spread modulation clock.

With regard to claim 3, the Examiner notes that Asada teaches a variable delay circuit and delays the chCLK to comply with a control input. The Examiner further notes that circuit 1422 detects a delayed state in the variable delay circuit and regulates the control input to the variable delay circuit. The Examiner asserts that this is done "in such a manner that a phase difference of the phase control clock to the reference clock does not exceed a specific limit value defined by the reference clock cycle as a unit." This latter language is not supported by any teaching in Asada et al, since there is no specific limit value described or even required by the circuit 1407. Thus, the Examiner again uses hindsight to create this basis for rejection. Moreover, for the reasons given previously, this dependent claim should be considered patentable.

With regard to claim 4, the Examiner again asserts that claim limitations exists in the teachings of Fig. 46, without support. In particular, the Examiner asserts that the control input is regulated "according to such a profile that the phase difference of the phase controlled clock to the reference clock [chCLK] gradually increases and gradually decreases between the upper limit and lower limit of the specific limit value defined by the reference clock cycle as a unit." Nothing of this sort is taught or even suggested in Asada et al or Lofgren et al. Thus, this claim should be considered patentable over the prior art.

Finally, with regard to claim 5, the Examiner asserts that Asada et al discloses a delayed lock loop (DLL) circuit containing the variable delay circuit 1425 as a circuit element wherein "the DLL circuit and the phase control means synthesize the control input to the variable delay circuitry". This claim would be patentable for the reasons given with regard to the claims from which they depend. .

Applicants appreciate the Examiner's indication of allowability of claim 6.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

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